A Review on Stability Estimation & Reduction in Power Consumption of 6T SRAM Cell

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ABSTRACT

SRAM Plays a major role for memory based applications in the range of large static noise margin. The noise present at the SRAM causes read and write's data stability. In this paper we are going to estimate the stability of the 6T SRAM while on the read and write mode of operation. While estimate this process we are analyzing the read, write margin for various supply voltages. The BL and write BITLINE carries the data at various VDD, VCELL. The leakage of this circuit from the N-MOS or P-MOS causes the low reliability, stability and also causes more power consumption. The 6T-SRAM with virtual ground is used to reduce the leakage from the transistor at the read and write operation. The data given to the circuit causes more stability and reliability for the high Static noise margin. The circuit is to designed at 45 nm CMOS process and analyzed in TANNER T-SPICE Simulations.

Keywords— 6T SRAM, Virtual ground, Stability.

INTRODUCTION

SRAM cell the power consumption is more due to leakage power. Technology scaling has led to increasing challenges in designing higher density static random-access memory (SRAM)[1]. In the past few decades, although 6T-SRAM cells have been the most common cell architecture, they are increasingly limited due to inherent device variations[2]. The increasing device fluctuation has made precise estimation of the SRAM-cell stability increasingly important[3]. Conventionally, SRAM yield is predicted either by a static-read margin or a write-noise margin (WNM)[4],[5].In stability estimation the most important factor is SRRV(supply read retention voltage), WTP(write trip voltage).by using that we can estimate the stability of cell. SRAM Plays a major role for memory based applications in the range of large static noise margin. The noise present at the SRAM causes read and writes operation delays. The level for this noise margin reaches
the ability of the read and write’s data stability. In this project the noise margin level and the stability of the 6T SRAM are going to estimate while on the read and write mode of operation. While estimate this process analyzing the read, write noise margin for various supply voltages. The BL and write BITLINE carries the data at various VDD, VCELL. Now a day’s in VLSI filed three factors are very important those are power, area and speed most of the engineers now concentrating on low power design in most of the electronics industry. In Most of the design the power consumption is more and speed also not good so these factors are very important in the major application one of the application is the memory design here power, speed & area play very important role.

**TYPES OF POWER CONSUMPTION**

A. Static power: Static power dissipation due to sub-threshold leakage, drain junction leakage and gate leakage due to tunneling. Among these, sub-threshold leakage is the most prominent one.

B. Dynamic power: dynamic power dissipation due to switching current from charging and discharging parasitic capacitance and another reason for dynamic power dissipation is shot-circuit current when both the n-channel and p-channel transistor are momentarily on at the same time. Power dissipation due to Switching current is 20 percent more than the power dissipation due to short circuit current. When technology feature size scales down, supply voltage and threshold voltage also scale down. Sub-threshold leakage power increases exponentially as threshold voltage decreases. Furthermore, the structure of the short channel device lowers the threshold voltage even lower. So it is becoming more and more important to reduce leakage power as well as dynamic power. There are several VLSI techniques for reducing leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit its application. In this project, we propose a virtual ground method to reduce the bit leakage power. We summarized and compared the previous techniques with new approach.

Lowering supply voltage is effective for power reduction because of the quadratic relationship between supply voltage and dynamic power consumption. To compensate the performance loss due to a lower supply voltage, transistor threshold voltage has to be decreased as well, which causes exponential increase in the sub-threshold leakage current. To reduce leakage power, multi threshold CMOS has been proposed with low blocks connected to ground through high transistors named as sleep transistors. The sleep transistor is turned on when the circuit is in the computational mode, and is turned off to cutoff the power supply in the standby mode for significant power reduction.

In order to achieve high performance and high density, the CMOS technology and threshold voltage scaled down from decades. Because of the scale down the technology the transistor leakage will increase exponentially. As the feature size becomes smaller, shorter channel lengths result in increased sub-threshold leakage current through a transistor when it is off. Low threshold voltage also results in increased sub-threshold leakage current because transistors cannot be turned off completely. For these reasons, static power consumption, i.e., leakage power dissipation, has become a significant portion of total power.
consumption for current and future silicon technologies. There are several VLSI techniques to reduce leakage power. Each technique provides an efficient way to reduce leakage power, but disadvantages of each technique limit the application of each technique. We propose a new approach, thus providing a new choice to low-leakage power VLSI designers. Previous techniques are summarized and compared with our new approach presented in this paper. So for improve the stability of SRAM cell use the virtual ground method because of these method not only reduce the power requirement but also minimize the delay.

CONVENTIONAL 6T SRAM CELL

1. Standby Mode (the circuit is idle)
In standby mode if word line (WL=0) then both the access transistor N3 & N4 will turn off and bit lines are completely disconnect with the inside latch circuit. The cross-coupled inverters will continue to force each other, in this mode the current drawn from supply voltage is called standby or leakage current.

2. Read Mode
In read mode for read 1 if WL=0 then both the access transistors N3 & N4 will turn off. Then pre-charged both the bit lines high and then make WL high WL=1. If A=0 & B=1 is stored then WL=1 causes N3 pass 0 to P2, N2 and N4 pass 1 or vdd to P1, N1. Charges flow from P2 to N4 charging the Bit_bar line voltage. Charges flow from N3 to N1 discharge the bit line voltage. Differential bit line voltages sensed by sense amplifier. Similarly in case of read 0 also.

3. Write Mode
For write 1 suppose initially there is 0 when the WL=0 then both the access transistor will off then pre-charged both the bit line to high Bit=1 and bit line bar to low Bit_bar=0. Now correct the WL=1 high then both the access transistor will turn on and the value of Bit line=1 will store in A and value of Bit_bar =0 will store in B. so, in that way write 1 operation performed. Similarly for write 0 also.

Figure 1 Schematic of 6t SRAM cell[6]
STABILITY ANALYSIS OF 6T SRAM CELL

For stability of the SRAM cell good SVNM is required so SVNM is the most important parameter for memory design. The higher SVNM of the cell confirms the high speed of SRAM. This work is to introduce how the signal to noise margin (SVNM), write trip voltage and write trip current of SRAM cell depends on the, cell ratio and pull-up ratio. In order to obtain high noise margin and less power dissipation new SRAM cell have been introduced. PR (pull-up ratio) and CR (cell ratio) and supply voltage are important parameters because these are the only parameters in the hand of the design engineers. Technology is getting more complex day by day so it should be carefully selected in design of the memory cell, there are number of design criteria that must be taken into consideration.

The two basic criteria which we have to taken such as

I] Data read operation should not destructive.
II] Static noise margin must be in acceptable range.

In this section, introduce existing static approaches for measuring read stability and write ability.

1 Read-Static-Noise-Margin and Write-Noise Margin:

Static noise margin (SNM) is a widely used term to quantify static logic’s stability in terms of the tolerable amount of dc noise voltage injected at the data storage nodes without changing the stored states. Read SNM (RSNM) and WNM are extended definitions of the SNM. These two terms are defined as the maximum tolerable noise that can be injected into the internal nodes of the SRAM cells without disturbing the intended operation. Despite the simple interpretation, the actual measurement of the RSNM and the WNM requires an internal node access of every single cell and graphical analysis on the measured data. Hence, the in situ measurement of these stability metrics is not realistic in a dense SRAM array. Due to the same issue, static voltage-noise margin and write trip voltage (WTV) from N-curve are not considered in this paper. As an alternative way of characterizing the SRAM cell’s read stability and write ability, supply read retention voltage (SRRV), and bit-line WTV (BWTV) are chosen that can be characterized by tracking the bit-line current with supply variation without the need to access the internal nodes.

2 Read Retention Voltage:

RRV is a measurable quantity for an in situ cell by changing the cell supply (SRRV) or word-line driver supply (WRRV). This discussion focuses on the SRRV as these two metrics are highly correlated. This technique can be used to extract the cell’s read stability without changing the cell layout. The approach measures the lowest cell supply voltage before disturbing the stored bit, all bit lines are tied to the supply line with the access transistors on, and the cell supply voltage (VCELL) is swept from high to low. At the beginning of the test, “0” is written into the target cell and hence VR stores a low state. Next, VCELL scales down by a predefined step V, and then the bit-line current (IBL) is measured. If the data are not changed, the nonzero amount of current can be measured. This procedure is repeated until the stored bit is flipped. At this cell supply level, IBL suddenly drops to zero. The amount of the supply voltage scaling is recorded as the SRRV.
3. Write Trip Voltage:
Similar to the concept of RRV, the write ability of a cell can be expressed as the marginal voltage of the BWTV or the WWTV during the write operation. As they are strongly correlated, we focus on the BWTV. The BWTV is defined as the maximum tolerable voltage on the low bit-line side for the successful writing of the wanted data bit. If the BLB voltage is not fully low, the internal state of the 6T cell will resist against the forced state reversal by the write access. The maximum tolerable nonzero bit-line voltage effectively represents how easily the cell can change its state during the write access and how the cell is robust against noise injected at the low-side bit line. Similar to the SRRV measurement, the BWTV can be measured without the change of the cell layout.

VIRTUAL GROUND
SRAM cells have been verified to work in the sub-threshold or near-threshold region. While decoupled SRAM cells improve the cell stability substantially during read operation, the stability of the half-selected cells is still a challenging issue. Pulsed word lines and hierarchical bit lines mitigate the stability degradation of the half-selected cells, but they degrade the write margin, demanding write margin improvement techniques. Therefore, design parameters and assisting circuits have to be carefully selected by tradeoffs. In ultra-low voltage SRAMs, leakage current occupies a substantial percentage of power and energy. Thus, energy aware leakage reduction is also important for the better energy efficiency.

A conventional 6T-SRAM cell design consists of a cross-coupled inverter pair (M3-M6) that does data storage and two access transistors (M1-M2) to load/retrieve data on bit lines, BL and BLB. During a write operation, the data is loaded on the bit lines and the word select signal WS is turned high. A successful write operation occurs if the data is correctly latched in the cell. The bit lines are pre-charged to the supply voltage and the word select line is turned high to retrieve data during a read operation. The bit line (BL) connected to the storage node (V1) storing a “0” gets discharged. The storage node (V1) rises above "0" during a read operation due to voltage division between the access transistor (M1) and the driver transistor (M6). A read failure can occur if the voltage drop rises higher than the threshold voltage of the inverter (M3,M5).

A conventional 6T-SRAM cell provides poor read stability since the access transistors provide direct access to the cell storage during a read operation. The proposed design removes the access hazard during a read operation and therefore eliminates the chances of cell content being inadvertently flipped. It consists of a cross-coupled pair (M3-M6) for data storage as in case of a conventional 6T-SRAM cell. However the ground terminal of the inverter pair is connected to a virtual ground (Gnd_vir1) in the proposed design to provide high speed low-power write operation. The word select line WS is held high only during a write operation to load new data in the cell by turning on the write access transistors (M1-M2). A read access transistor (M7) connected to a virtual ground (Gnd_vir2) is used to retrieve data on read bit line (BLR) during a read operation. Our design decouples read/write operation using separate read/write access transistors. Therefore it doesn’t suffer from constrained read/write requirements as in 6T-SRAM design.
CONCLUSION

Virtual grounding is best method for reduction of leakage current. It is also useful for reduction of noise. And because of these SRAM cell become more stable. Delay in read and swrite operation also overcome by these method. These method is very useful in low power design.

REFERENCES