Design of SD Host Controller For On An ALTERA DE2 Board

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ABSTRACT
A Secure Digital Host Controller(SDHC) in which FIFO concept is used and it is developed in verilog language in Altera Quartus II 10.0 environment and the system clock is generated by using a clock divider and it is implemented on the ALTERA DE2 Board system is designed which consumes low power and it transfers data without any data loss with greater speed. Using Altera SOPC (SYSTEM-ON-A-PROGRAMMABLE-CHIP) Builder with the NIOS II system, in which the Altera DE2 board will support communication through the SD card. These features are realized using Altera SOPC builder in the Altera Quartus 10.0 tool. The overall goal of this project is to explore various applications that are possible with Altera’s DE2 Board.

Keywords— AlteraDE2 board, SD card , SDHC, NIOS II processor, SOPC builder.

1. INTRODUCTION
With the increasing consumer digital content, demand for high capacity digital storage has increased rapidly. SD Card (Secure Digital Card) is a nonvolatile memory card used extensively in portable devices, such as mobile phones, digital cameras, GPS navigation devices, handheld consoles, and tablet computers. It is a family of solid-state storage media. SD Card is an ultra small flash memory card designed to provide high-capacity memory in a small size. SD cards are used in many small portable devices such as digital videocamcorders, digital cameras, handheld computers, audio players and mobile phones. Different memory formats like Flash, Secure Digital (SD), Compact Flash, Universal Serial Bus(USB), and Multimedia Card (MMC) are available in the market to store the digital contents. Portable devices are battery operated, so they need to be power efficient [1],[8].

The SDHC standard was developed by the Secure Digital Association (SDA) which addresses the requirement to support the growth in storage capacity of memory cards. A regular SD card which is the first version of the standard, limits its
maximum storage capacity [8]. SDHC cards is used as a later version of the standard, which can store more data and also support ultra high-speed data transfer rates that a regular SD card does not support. A regular SD card uses the first version of the standard, which limits its maximum storage capacity. SDHC cards, which use a later version of the standard, can store more data and may also support ultra high-speed data transfer rates that a regular SD card does not support.

Secure digital is a non-volatile memory card format developed and managed by Secure Digital Association. SDHC Card is a semiconductor flash based memory device which is well known for its simple interface, high bandwidth, low cost, greater security, low power etc[4]. This article discusses in detail, the implementation of the FIFO and Clock divider using SOPC builder, NIOS II processor and Altera DE2 board.

2. BACKGROUND WORK

A novel neuro-fuzzy control approach is adopted to reduce the burstiness of the traffic-shaping buffer output rate frame by frame to enable the VBR encoded video to enter the Bluetooth network, the two objectives it mainly focussed on to smooth the traffic congestion and to maintain constant video quality. The main advantages are having maximum achievable speed with the available resources and the data transfer rate is high.

Video over wireless communication (VoW) has a lot of potential applications in home and office environment. Bluetooth and MPEG-4 is used in implementing VoW. Video transmission over wireless channel can transmit MPEG-4 bit streams over Bluetooth channels. This paper presents the implementation details of MPEG-4 coded video transmission over Bluetooth (MPEG4BT) via Host Controller Interface (HCI).data partitioning does improve in video playback performance. Advantages of VOW achieves higher compression rate and the video quality is obtained good despite the Bluetooth bandwidth limitation.

High Performance FPGA-Based DMA Interface for PCIs design has been optimized in this article focus on increasing package sizes are of the order of 11kB. With larger package sizes, the performance increased. DMA, produces measured transfer speeds up to 748 MB/s (read) and 784 MB/s (write) using the Xilinx VC707 Virtex-7 board and advantages in this article is its Bluetooth permits high-quality, high-security, high-speed, and low-power voice and data transmission and the drawback is it requires high bandwidth.

The PCI Express Solid State Drives (PCIe SSDs) blur the difference between block and memory access semantic devices. In this work, it analyzed the challenges PCIe SSDs face in getting flash memory closer to the CPU side, and study two representative PCIe SSD architectures and flash software stacks .The experimental analysis reveals that the future PCIe SSD architectures need to redesign the current data paths from CPU to flash memories by removing redundant I/O protocols and flash controllers. Their flash software should address the dramatic performance drops caused by multi-core systems, storage-level queuing mechanism, and flash garbage collection. PCIe SSD architectures and software modules need to
manage dynamic power more efficiently as they require more power than a high-end conventional SSD by 200% to 500%.

Compact Flash or USB flash memory drives can be implemented without paying for licensing, royalties, or documentation. Compact Flash and USB flash drives may require licensing fees for the use of the SDA’s trademarked logos.

3. SD HOST CONTROLLER

SDHC cards are memory cards in which are used to store files, music, pictures, video and any other data. SDHC cards are supported by many small electronic devices that use memory cards for storage. A regular SD card uses the first version of the standard, which limits its maximum storage capacity. SDHC cards are used as a later version of the standard, can store more data, supports ultra high-speed data transfer rates than a regular SD card. Secure digital Card, which is a non-volatile memory card format developed and managed by Secure Digital Association (SDA). The SD3.0 Host Controller is a Host Controller with an ARM processor interface and belongs to SD Host Controller Standard Specification Version 3.00. The block diagram of SD Host Controller is shown below in Figure 1.

Figure 1. The Block Diagram of SD Host Controller

SDHC has internal FIFO can perform both read and write transactions. The Host Processor can access the various registers and FIFO in the Host Controller to transfer data between Host and SD Card. It enables the host to access SD Devices such as SD Memory Cards, SDIO devices, SD Combo devices etc[1-3].

The SD Protocol operates as a Master-Slave communication model. It employs a command-response mechanism. Commands are always initiated by the Host Controller and responded to by the Card. The Host Controller has two interfaces the System side interface and the SD Bus interface. The Host Driver is on
system bus time and the SD Card is on SD Bus time. The Host Controller assumes that both these interfaces are asynchronous as in [5].

3.1 Data FIFO
The SD/SDIO Host Controller uses 1k dual port FIFO(First In First Out) for performing both read and write transactions. FIFO is linear Queue mode of operation[1]. Two address pointers are used to define the head and the tail of the FIFO. FIFO is defined to be full when the head pointer and the tail pointer are equal. During a write transaction (data transferred from Processor to SD3.0 card), the data will be filled in to the first and second half of the FIFO alternatively. When data from first half of FIFO is transferring to the SD3.0 card, the second half of FIFO will be filled and vice versa. The two halves of the FIFO’s are alternatively used to store data which will give maximum throughput. During a read transaction (data transferred from SD3.0 card to Processor), the data from SD3.0 card will be written in to the two halves of the FIFO alternatively. When data is from one half of the FIFO is transferring to the Processor, the second half of the FIFO will be filled and vice versa and achieves the throughput to be maximum. If the Host controller cannot accept any data from SD3.0 card, then it will issue read wait to stop the data transfer from card or by stopping the clock[1].

3.2 Data Control Logic
The DAT [0-7] control logic block is used to transmit data on the data lines during write transaction and receives data from the data lines during read transaction. The DAT [0-7] control logic block transmits data in the data lines on posedge and negedge of the SD Clock [1]. The DATA [0-7] receiver block receives/samples the data on the data lines in both posedge and negedge of the SD Clock. The Command control logic block sends the command on the command line and receives the response coming from the SD3.0 card [1],[5].

3.3 Clock Divider Logic
A clock divider, also called a frequency divider is a circuit that takes an input signal of a frequency and it generates an output signal of a frequency. The Clock generation block is used to divide and enable/disable the SD clock. It consists of a Clock Divider and state register. The Clock Divider is a loadable counter. A new value is written to the state register. Count register is set, the Clock Divider starts to count down from the loaded value to ‘0’to ‘15’.The clock controls SD clock toggling.

4. SOPC BUILDER
SOPC (SYSTEM-ON-A-PROGRAMMABLE-CHIP) BUILDER is a powerful system development tools used to create systems based on processors, peripherals, interfaces and memories. It is embedded with a library of built-in components such as a Nios II soft processor, memory controllers, interfaces, standard peripherals custom peripherals. In SOPC Builder, the system components are routed in a GUI (Graphical User Interface). The GUI is exclusive in configuring the soft-hardware components and it acts as a
general-purpose tool for creating systems that includes a soft processor apart from the Nios II processor. SOPC Builder is implemented for the purpose of generating a complete SOPC by consuming less time than the accustomed integration methods [9]. Altera has SOPC Builder functionality built in Quartus II, which accordingly connects the soft-hardware components to construct a complete computer system that can be controlled on any of the FPGA chips and also capable of producing interconnect. It contributes to writing software and system simulation [9].

4.1 Core Functionalities of SOPC Builder

It has four functions includes:

- Describes the hardware of the system.
- Performs the system generation.
- Performs memory mapping for initiating the software development.
- Produces test bench to simulate the design.

4.2 Architecture and Design of SOPC Builder

Designs using SOPC Builder are generated to develop a top level HDL (hardware description language) file by connecting various modules together. These various modules are considered the building blocks for the SOPC Builder system [9].

For the connection of multiple components in the system, the modules use Avalon (Avalon switch interconnect) interfaces, such as memory-mapped, streaming and IRQ (interrupt request) as in [9].

4.3 SOPC Design Flow

The design flow of SOPC Builder is as follows:

Add components by Component Editor.

Initiate Simulation of the system.

Develop the system design by adding components, Interrupt Request (IRqs) and addresses.

Start the system generation.

Conduct system level simulation.

Compile the system design.

Download .sof file to an Altera FPGA.

4.4 NIOS II PROCESSOR

Nios II is a 32-bit soft-core embedded processor architecture designed specifically for the Altera family of FPGAs. The Nios II processor is a configurable soft-core processor that allows features to be added or removed on a system-by-system basis to meet performance requirements. On this single Altera chip or Nios II processor core the user can implement both peripherals and memory.
5. RESULTS AND DISCUSSIONS

In this section, mainly discussed about the simulation results, synthesis report and the final hardware implementation of Audio and results are described below. The FIFO Block has been implemented in Altera Quartza Synthesize tools using verilog code. The FIFO concept is used in memory block of SD Host Controller as shown in Figure 5.1(a).

![FIFO_BLOCK](image1)

**Figure 5.1 (a) RTL Schematic of FIFO Block**

FIFO operates based upon the clock pulse and state machine if the memory reaches the 15 address then it shows empty as low and full as high and if it reaches initial zero it is vice versa and it is shown in the Figure

![FIFO_BLOCK](image2)

**Figure 5.1 (b) Output Waveform of FIFO Block**

The clock divider circuit had designed for system clock which has the frequency of 50MHz. The Clock Divider is a loadable counter Based upon the loadable 8 bit counter, the clock toggles from high to low and vice versa and it adds new value to a state register as shown in the Figure 5.2 (a).

![newdiv](image3)

**Figure 5.2 (a) RTL Schematic of Clock Divider Block**
Figure 5.2 (b) The output waveform of Clock divider integrated block

A new value is written to the state register. Count register is set, the Clock Divider starts to count down from the loaded value to ‘0’ to ‘15’. The clock controls SD clock toggling. The clock divider circuit is the top module and the counter block was integrated as sub module to clock divider block and it is synthesized using the Modelsim. The output waveform of Clock divider integrated block is shown in the Figure 5.2 (b).

Figure 5.3 Pin Assignment Editor

The above integration clock divider block is analyzed and it is checked for errors and after the design is checked successfully with no errors. The pin location is assigned using pin assignment editor as shown in the Figure 5.3.

The Top module Clock Divider project is exported as .csv file and saved in the file and exported in the Pin Assignment Editor as in the Figure 5.4.
The Top module Clock Divider project is exported and the full design should be compiled. Compile the design and design is compiled successfully as shown in the Figure 5.5.

The project has to be programmed to the ALTERA Board. The program is implemented in hardware is created as .sof file as shown in the Figure 5.6.
Then the hardware setup had to be done by connecting the USB Blaster of ALTERA Board to the system. Add the USB Blaster and finish it. Then select the .sof program file and start to program it and it takes a time for loading the program. After the program is loaded successfully and it is loaded to the FPGA Board as shown in the Figure 5.7.

Thus the clock divider module with counter had been designed and implemented on an Altera Board and the counter output can be viewed till it reaches 11111111 as in below Figures 5.8(a),(b).
FIFO AND CLOCK DIVIDER CIRCUIT IMPLEMENTATION USING ALTERA DE2 BOARD

SOPC Builder is initialized and to choose the language (verilog or vhdl) is the code generated as shown in the Figure1 . Many other components as timers, inputs, outputs, can be added and personal components and interfaces can be created using SOPC builder.

![Figure 1. SOPC BUILDER](image1)

The ALTERA SOPC Builder generates the Nios II processor system, adding other peripherals as shown in the Figure 2.

![Figure 2. The NIOS II E Processor.](image2)

The JTAG Uart provides a way to communicate the processor through the USB-Blaster. For initialize JTAG UART, in component library select interface protocols select serial and Click on JTAG UART. After JTAG UART is added and click on the system generation, you can download the design onto a board, and debug the software executing on the board as shown in the Figure 3. The Project has to be programmed to the ALTERA Board. The program is implemented in hardware is created as .sof file as shown in the Figure 3.

![Figure 3. Programmer Setup](image3)
Then the hardware setup had to be done by connecting the USB Blaster of ALTERA Board to the system. Add the USB Blaster and finish it. Then select the .sof program file and start to program it and it takes a time for loading the program. After the program is loaded successfully and it is loaded to the FPGA Board as shown in the Figure 5.

Figure 4. Hardware Setup of USB Blaster

Once the program running on the Nios II processor is started, it will detect the existence of the USB mouse connected to DE2-115 board in [4].

CONCLUSION

The main goal of this study was to design a SD Host Controller in which FIFO concept is generated in verilog file and the system clock is generated by using a clock divider and because of data FIFO, it transfers data without any data loss. Using the Nios II E displays initially the SD CARD, a data stream of 512 bytes is moved from the SD card onto the FIFO (First-In First-Out) Buffer and it is implemented on the ALTERA DE2 Board system SD host controller mainly achieves high speed, low power.

REFERENCES

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