EFFECT OF LEAKAGE CONTROL TRANSISTOR TECHNIQUE ON COMBINATIONAL CIRCUITS

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ABSTRACT

Due to integration of millions of components and shrinking process technology, nowadays leakage power tends to play a major role in total power consumption. LECTOR, a technique to tackle the leakage problem in CMOS circuits, uses two additional leakage control transistors. The main advantage as compared to other techniques. The LECTOR technique does not require any additional control and monitoring circuitry, thereby limits the power dissipation in active state. The half adder, full adder and multiplexer circuits are designed using LECTOR in 32nm CMOS technology and their performances are analysed.

Keywords- Power Dissipation, leakage control transistor, CMOS technology.

INTRODUCTION

Leakage power of a CMOS transistor depends on gate length and oxide thickness [4]. To decrease the dynamic power, the supply voltage is decreased which leads to the performance degradation. To speed up the device, the threshold voltage should also be scaled down along with the supply voltage, which results in exponential increase in the sub-threshold leakage current, thereby increase in the static power dissipation. For the rapid increase in power consumption of present day chips, the innovative cooling and packaging strategies are of little help. Also, the cost associated with the packaging and the cooling of such devices is becoming prohibitive. In addition to cost, the issue of reliability is a major concern. Component failure rate roughly doubles for every 100c increase in operating temperature. With the on-chip devices doubling every two years, minimizing the power consumption has become currently an extremely challenging area of
research [1]. Increase in the transistor speed and number of transistors result in high performance in the current generation processors. The performance improvements have been accompanied by an increase in the power dissipation. High power dissipation systems increase cost of cooling and reduce the system reliability. The advantage of utilizing a combination of low-power components in conjunction with low-power design techniques is more valuable now than ever before. Requirements for lower power consumption continue to increase significantly as components become battery-powered, smaller and require more functionality. Motivations for reducing power consumption differ application to application. Power consumption due to leakage has joined switching activity as a primary power management concern. There are many techniques that have been developed over the past decade to address the continuously aggressive power reduction requirements of most of the high performance.

Ravi .T et al. describes about the high performance double edge triggered D flip flop [9].

LECTOR TECHNIQUE

The effective stacking of transistors in the path from supply voltage to ground is the basic idea behind the LECTOR technique for the leakage power reduction. This is stated based on the observation from [2] and [5] that “a state is far less leaky with more than one OFF transistor in a path from supply voltage to ground compared to a state with only one OFF transistor in the path”. Two LCTs are introduced between nodes N1 and N2. The gate terminal of each LCT is controlled by the source of the other, hence termed as self-controlled stacked transistors. As LCTs are self-controlled, no external circuit is needed, thereby the limitation with the sleep transistor technique has been overcome. The introduction of LCTs increases the resistance of the path from Vdd to Gnd, thus reducing the leakage current.

Leakage Control Transistor (LECTOR) technique is illustrated in the figure 1. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively. This connection always keeps one of the two LCTs in its near cut-off region for any input.

Figure 1. LECTOR technique
DESIGN OF DIGITAL CIRCUITS USING LECTOR

The digital circuits are designed using LECTOR technique are explored in this section.

A. AND GATE

In an AND gate the LECTOR technique is applied between the pull up and pull down networks as shown in Figure 2. The source nodes of LCT1 and LCT2 are the nodes N1 and N2 respectively of the pull-up and the pull-down logic. The gates of LCT1 and LCT2 are controlled by the potential at source terminal of LCT2 and LCT1 respectively.

![Figure 2 AND Gate using LECTOR technique](image)

A. HALF ADDER

The half-adder is a digital circuit which adds two input bits and generates a carry and sum, which are the two outputs of half-adder as shown in Figure 3.

![Figure 3. Half adder](image)

The LECTOR implementation here needs only two additional transistors to be placed between the pull-up and pull-down network at the node from which the output is taken.
B. FULL ADDER

Full Adder is a combinational circuit that performs addition of three bits. It consists of three inputs and two outputs. The Gate level schematic of Full Adder is shown in Figure 4. The LECTOR implementation involves the addition of two LCTs for each gate.

![Figure 4. Full adder](image)

C. MULTIPLEXER

The gate level schematic of 2:1 multiplexer is shown in Figure 5. The LECTOR implementation involves the addition of two LCTs in each gate between the supply and ground path.

![Figure 5. Multiplexer circuit](image)

1. TRANSIENT ANALYSIS

To evaluate the performance of LECTOR based half adder, full adder and multiplexer circuit discussed in this paper are designed using 32-nm CMOS technology. All simulations are carried out using HSPICE simulation tool. Figure 6, 7 and 8 represents the simulation results of the above mentioned circuits.
Figure 6 Simulated Results of multiplexer circuit using LECTOR Technique
In the above analysis v(4) is the selection line, v(5),v(6) are input signals and v(30) is the output signal.

Figure 7 Simulated Results of half adder circuit using LECTOR Technique
In the above analysis v(2),v(3) are input signals and v(4),v(5) are output signals.

Figure 8 Simulated Results of full adder circuit using LECTOR Technique
In the above analysis v(4),v(5) and v(6) are input signals and v(46),v(86) are output signals.

2. PERFORMANCE ANALYSIS
The average power and leakage power of LECTOR based half adder, full adder and multiplexer circuits are obtained and analysed.

Table 1 POWER ANALYSIS OF HALF ADDER

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>Average power (W)</th>
<th>leakage power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVENTIONAL DESIGN</td>
<td>9.53 x10^{-6}</td>
<td>1.63 x10^{-06}</td>
</tr>
<tr>
<td>LECTOR</td>
<td>7.19 x10^{-07}</td>
<td>42.3x10^{-12}</td>
</tr>
</tbody>
</table>
Table 1 describes the power analysis of conventional and lector based half adder circuit using 32nm CMOS technology.

Table 2 POWER ANALYSIS OF FULL ADDER

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>Average power (W)</th>
<th>leakage power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVENTIONAL</td>
<td>8.49 x10^{-05}</td>
<td>66.64 x10^{-09}</td>
</tr>
<tr>
<td>DESIGN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LECTOR</td>
<td>1.96 x10^{-06}</td>
<td>23.49 x10^{-09}</td>
</tr>
</tbody>
</table>

Table 2 describes the power analysis of conventional and lector based full adder circuit using 32nm CMOS technology.

Table 3 POWER ANALYSIS OF MULTIPLEXER

<table>
<thead>
<tr>
<th>DESIGN</th>
<th>Average power (W)</th>
<th>leakage power (W)</th>
</tr>
</thead>
<tbody>
<tr>
<td>CONVENTIONAL</td>
<td>9.51 x10^{-05}</td>
<td>9.86 x10^{-09}</td>
</tr>
<tr>
<td>DESIGN</td>
<td></td>
<td></td>
</tr>
<tr>
<td>LECTOR</td>
<td>6.51 x10^{-05}</td>
<td>6.67 x10^{-09}</td>
</tr>
</tbody>
</table>
Table 3 describes the power analysis of conventional and lector based multiplexer using 32nm CMOS technology.

CONCLUSION
As technologies have shrunk, leakage power consumption has grown exponentially, thus requiring more aggressive power reduction techniques. LECTOR technique achieves the reduction in leakage power since this technique does not require any additional control circuitry and the exact logic state is maintained. From the above analysis the digital circuits which claims that the LECTOR technique based digital circuits achieves up to 80-85% leakage reduction over the respective conventional circuits without affecting the dynamic power.

ACKNOWLEDGEMENT
I take this opportunity to express my profound gratitude and deep regards to my internal guide and Assistant Professor Mr. T. Ravi for his exemplary guidance and constant encouragement during the project period. Next, I would like to extend my deep gratitude to the principal of Jeppiaar Institute of Technology Dr. V. Kannan for his timely help and guidance and I offer my sincere thanks to Assistant Professor Mr. N. Mathan for constant support during the period of my project work.

REFERENCES


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