Power Optimization of Single-Phase Clock Multiband Flexible Divider

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ABSTRACT
In this paper, a power optimization of single phase multiband flexible divider is proposed for the networks like Zigbee, Bluetooth, Wireless LAN, IEEE 802.15.4 and 802.11a/b/g. In this paper, a wideband 2/3 and 4/5 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 prescaler and 64/65/79/80 prescaler. A dynamic logic multiband flexible integer-N divider is designed which uses the wideband 4/5 prescaler, multimodulus 32/33/47/48 prescaler and 64/65/79/80 prescaler. Since the multimodulus 32/33/47/48 prescaler and 64/65/79/80 prescaler has maximum operating frequency of 6.2 GHz, the values of P and S counters can actually be programmed to divide over the whole range of frequencies. However, the P and S counters are programmed accordingly. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow - counter and consumes a power of 0.96 and 2.2 mW, respectively, and provides a solution to the low power PLL synthesizers for the networks named earlier with variable channel spacing.

Keywords- Prescaler, Wireless LAN, Multimodulus Prescaler, Single phase clock

INTRODUCTION
WLAN in the gigahertz bands, such as Zigbee and IEEE 802.11a/b/g, are recognized as familiar standards for high data rate transmissions, and standards like IEEE 802.15.4 are recognized for low data rate transmissions[1]. The demand for small size, lower power, and multiband RF circuits increased in conjunction with need of higher level of integration. The frequency synthesizer, usually implemented by a Phase-Locked Loop (PLL), is one of the power-hungry blocks in the RF front-end and the stage-I frequency divider.

The high-speed frequency divider is a key block in frequency synthesis. The prescaler is the most challenging part in the high-speed frequency-divider design because it operates at the highest input
A dual-modulus prescaler usually consists of a divide-by-2/3 (or 4/5) unit followed by several asynchronous divide-by-2 units. The operation of the divide-by-2/3 unit at the highest input frequency makes it the bottleneck of the prescaler design. To achieve the two different division ratios, D Flip-Flops (DFFs) and additional logic gates, which reduce the operating frequency by introducing an additional propagation delay, are used in the unit [1]. The power consumption of this divide-by-2/3 unit, which is the greatest portion of the total power consumption in the prescaler, significantly increases due to the power consumption of the additional components.

Consumes a large portion of power in a frequency synthesizer. Dynamic latches are faster and consume less power compared to static dividers [2]. The frequency synthesizer reported in uses a prescaler as the first-stage divider, but the divider consumes Power. Most IEEE 802.11a/b/g frequency synthesizers employ SCL dividers as their first stage, while dynamic latches are not yet adopted for multiband synthesizers. In this paper, a dynamic logic multiband flexible integer-N divider based on pulse-swallow topology is proposed which uses a low-power wideband 2/3 and 4/5 prescaler and a wideband multi modulus 32/33/47/48 prescaler and 64/65/79/80 prescaler [2]. The divider also uses an improved low-power loadable bit-cell for the Swallow S counter.

The frequency synthesizer is one of the basic building blocks in modern communication systems. The operating frequency of the frequency synthesizer is limited by the frequency divider and the Voltage-Controlled Oscillator. The function of channel selection in the frequency synthesizer demands programmable division ratios for the frequency divider [3]. The integer-N frequency synthesizer is more practical, less costly and of low spurious sideband performance as compared with the fractional-N frequency synthesizer. It is usually formed by a prescaler, a Program Counter (P counter) and a Swallow Counter (S counter). Such a topology can provide a programmable division ratio of NP + S, where N, P and S are the division ratios of three blocks respectively [3]. The prescaler provides a dual-modulus of N=N+1.

**METHODOLOGIES**

The key parameters of high-speed digital circuits are the propagation delay and power consumption [4]. The maximum operating frequency of a digital circuit is calculated.

\[
F_{\text{max}} = \frac{1}{(tp_{\text{LH}} + tp_{\text{HL}})}
\]  

(1)

where \(tp_{\text{LH}}\) and \(tp_{\text{HL}}\) are the propagation delays of the low-to-high and high-to-low transitions of the gates, respectively. The total power consumption of the CMOS digital circuits is determined by the switching and short circuit power. The switching power is linearly proportional to the operating frequency and is given by the sum of switching power at each output node as in

\[
P_{\text{switching}} = \sum_{k=1}^{n} f_c L_k V_{dd}^2
\]  

(2)
Where \( n \) is the number of switching nodes, \( F_{\text{clk}} \) is the clock frequency, \( CL_i \) is the load capacitance at the output node of the \( i \)th stage, and \( V_{\text{dd}} \) is the supply voltage [4]. Normally, the short-circuit power occurs in dynamic circuits when there exists direct paths from the supply to ground which is given by

\[
P_{sc} = I_{sc} \times V_{dd}
\]  

(3)

Where \( I_{sc} \) is the short-circuit current. The analysis shows that the short-circuit power is much higher in E-TSPC logic circuits than \( n \) TSPC logic circuits [5]. However, TSPC logic circuits exhibit higher switching power compared to that of E-TSPC logic circuits due to high load capacitance. For the E-TSPC logic circuit, the short-circuit power is the major problem [5]. The E-TSPC circuit has the merit of higher operating frequency than that of the TSPC circuit due to the reduction in load capacitance, but it consumes significantly more power than the TSPC circuit does for a given transistor size. The following analysis is based on the latest design using the popular and low-cost 0.18-microm CMOS process.

**WIDEBAND SINGLE-PHASE CLOCK 2/3 PRESCALER**

The E-TSPC 2/3 prescaler reported in consumes large shortcircuit power and has a higher frequency of operation than that of 2/3 prescaler. The wideband single-phase clock 2/3 prescaler used in this design was reported which consists of two D-flip-flops and two NOR gates embedded in the flip-flops as in Fig. 1. The first NOR gate is embedded in the last stage of DFF1, and the second NOR gate is embedded in the first stage of DFF2 [6]. Here, the transistors M2,M25, M4, and M8 in DFF1 helps to eliminate the short-circuit power during the divide-by-2 operation. The switching of division ratios between 2 and 3 is controlled by logic signal MC.

![Fig. 1 Wideband Single-Phase Clock 2/3 Prescaler](image)

When MC switches from “0” to “1,” transistors M2, M4 and M8 in DFF1 turns off and nodes S1, S2 and S3 switch to logic “0.” Since node S3 is “0” and the other input to the NOR gate embedded in DFF2 is \( Q_b \), the wideband prescaler operates at the divide-by-2 mode[6]. During this mode, nodes S1, S2 and S3 switch to logic “0” and remain at “0” for the entire divide-by-2 operation, thus removing the switching power contribution of DFF1. Since one of the transistors is always OFF in each stage of DFF1, the short-circuit power in DFF1 and the first stage of DFF2 is negligible. The total power consumption of the prescaler in the divide-by-2 mode is equal to the switching power in DFF2 and the short-circuit power in second and third stages of DFF2.
Where CLi is the load capacitance at the output node of the ith stage of DFF2, and Psc1 and Psc2 are the short-circuit power in the second and third stages of DFF2. When logic signal MC switches from “1” to “0,” the logic value at the input of DFF1 is transferred to the input of DFF2 as one of the input of the NOR gate embedded in DFF1 is “0” and the wideband prescaler operates at the divide-by-3 mode. During the divide-by-2 operation, only DFF2 actively participates in the operation and contributes to the total power consumption since all the switching activities are blocked in DFF1. Thus, the wideband 2/3 prescaler has benefit of saving more than 50% of power during the divide-by-2 operation.

**MULTIMODULUS 32/33/47/48 PRESCALER**

The proposed wideband multimodulus prescaler which can divide the input frequency by 32, 33, 47, and 48 is shown in Fig. 2. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer [7]. The proposed prescaler performs additional divisions (divide-by-47 and divide-by-48) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider which will be discussed in Section V. The multimodulus prescaler consists of the wideband 2/3 \((N1/(N+1))\) prescaler [10], four asynchronous TSPC divide-by-2 circuits \((AD)=16\) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling \(N(N+1)\) divisions, the additional control signal \(Scl\) is used to switch the prescaler between 32/33 and 47/48 modes.

Case 1: Sel='0'

When Sel=0, the output from the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as the normal 32/33 prescaler, where the division ratio is controlled by the logic signal MOD. If MC=1, the 2/3 prescaler operates in the divide-by-2 mode and when MC=0, the 2/3 prescaler operates in the divide-by-3 mode.

If MOD =1, the NAND2 gate output switches to logic “1”(MC=1) and the wideband prescaler operates in the divide-by-2 mode for entire operation. The division ratio N performed by the multimodulus prescaler is

\[
N = (AD*N1)+(0*(N1+1)) = 32
\]
Where $N=2$ and $AD=16$ is fixed for the entire design. If $MOD=0$, for 30 input clock cycles $MC$ remains at logic “1”, where wideband prescaler operates in divide-by-2 mode and, for three input clock cycles, $MC$ remains at logic “0” where the wideband prescaler operates in the divide-by-3 mode. The division ratio $N+1$ performed by the multimodulus prescaler is

$$N + 1 = ((AD - 1)*N1)+(1*(N1+1)) = 33 \quad (5)$$

Case 2: $Sel = 1$

When $Sel = 1$, the inverted output of the NAND2 gate is directly transferred to the input of 2/3 prescaler and the multimodulus prescaler operates as a 47/48 prescaler, where the division ratio is controlled by the logic signal $MOD$. If $MC = 1$, the 2/3 prescaler operates in divide-by-3 mode and when $MC=0$, the 2/3 prescaler operates in divide-by-2 mode which is quite opposite to the operation performed when $Sel=0[8]$.

If $MOD = 1$, the division ratio $N+1$ performed by the multimodulus prescaler is same as except that the wideband prescaler operates in the divide-by-3 mode for the entire operation given by

$$N + 1 = ((AD * (N1+1))+(0*N1)) = 48 \quad (6)$$

If $MOD = 1$, the division ratio $N$ performed by the multimodulus prescaler is

$$N = ((AD - 1) \cdot (N1+1)) + (1*N1) = 47 \quad (7)$$

4.1 $4/5$ Prescaler

The 4/5 prescaler reported in consumes large short circuit power and has a higher frequency of operation than that of 4/5 prescaler. The wideband single-phase clock 4/5 prescaler used in this design, which consists of three D-flip-flops and two Nand gates embedded.

The Multi prescaler 4by5 consist of four D-flip flop, two Nand gates, and two OR gates one Not gate with main 4/5 prescaler circuit. The multi modulus prescaler operates as the normal 64/65/79/80.

4.2 Multiprescaler_4/5

The proposed wideband multimodulus prescaler which can divide the input frequency by 64, 65, 79 and 80 is shown in Fig. 4. It is similar to the 32/33 prescaler used in, but with an additional inverter and a multiplexer. The proposed prescaler performs additional divisions (divide-by-79 and divide-by-80) without any extra flip-flop, thus saving a considerable amount of power and also reducing the complexity of multiband divider. The multimodulus prescaler consists of the wideband 2/3 ($N1/(N+1)$) prescaler, four
asynchronous TSPC divide-by-2 circuits ((AD)=16) and combinational logic circuits to achieve multiple division ratios. Beside the usual MOD signal for controlling N/(N+1) divisions, the additional control signal Sel is used to switch the prescaler between 64/65 and 79/80 modes.

![Fig. 4. Multiprescaler_4by5](image)

Our proposed multiband flexible divider is combined by 2/3 Prescaler and 4/5 Prescaler in multi modulus Prescaler is shown in Fig.5. By using mux we can operate either 2/3 Prescaler and 4/5 Prescaler. It will operate 32/33/47/48 or 64/65/78/79 bandwidth.

### 4.3 Program Counter

The program counter is responsible for counting P pulses of Slow CLK before outputting a pulse to the phase/frequency detector and resetting itself and the swallow counter. The implementation used in this project, using a 7-bit ripple counter, a 7-bit comparator, and a zero-detector is shown in Figure.6. The ripple counter is clocked by SlowCLK, and increments its count by one each clock cycle. At each stage, the 7-bit comparator compares each count bit to the corresponding bit in the control signal, and outputs a 0 for each equal bit. When the zero-detector detects equivalence in all of the 7 bits, indicating that the desired count has been reached, Fout is driven high. On the next clock cycle, the program counter is reset to zero and the count
is restarted. In addition, the output pulse on Fout is used to reset the count of the swallow counter, indicating the end of one complete cycle of the frequency divider.

![Fig.6. Block Diagram of a 7-Bit Program Counter](image_url)

The ripple counter is implemented using 7 cascaded D-type flip-flops, each arranged in a toggle configuration. The output of each flip-flop is used to clock the next flip-flop. Since the output of each flip-flop inverts on every clock cycle, each flip-flop essentially divides its clock by two, causing the next stage of the ripple counter to be clocked at half the rate of the previous flip flop. Each flip-flop was designed to respond to the falling edge of its clock, when the output of the previous stage changes from a 1 to a 0. In this way, an incrementing binary count is achieved with the outputs of each flip-flop forming the bits of the count. Since the program counter contains 7-bits, any count between 0 and 127 can be set by the control signal. It is important to realize however that in order to achieve a division ratio as specified in the equation $DIV=NP+S$, the control signal must be set to $P-1$, since the zero-state is included in the count.

### 4.4 Swallow Counter

The swallow counter, as indicated in Figure.7, is used to count $S$ pulses of Slow CLK before asserting the modulus control signal and changing the modulus of the DMP to $N$. The similarities between the swallow counter and the program counter are apparent. Once again, the count (6-bits in this case) is maintained using a ripple counter comprised of cascaded flip-flops clocked with SlowCLK. In addition, a comparator compares each count bit with its corresponding bit in the control signal, and a zero-detector asserts modulus control when all bits are equal. However, the swallow counter does not reset when the count is reached, but masks the input clock using an AND gate connected to the inverse of modulus control. As a result, the ripple counter stops counting when the count is reached, and the state of the circuit is maintained until a reset signal (SwallowRST) is received from the program counter. Since the swallow counter contains 6 bits, it is capable of any count from 0 to 64. Once again, the control signal must be set to $S-1$, since the zero-state is included in the count.
**Fig 7.** Block Diagram of a 6-Bit Swallow Counter

**SIMULATION RESULTS**

![Simulation Results](image)

**Fig. 8 Frequency Divider 2/3**
CONCLUSION

In this paper, a wideband 2/3, 4/5 prescaler is verified in the design of proposed wide band multimodulus 32/33/47/48 and 64/65/79/80 prescaler. A dynamic logic multiband flexible integer N divider is designed which uses the wideband 2/3 prescaler, multimodulus 32/33/47/48 prescaler, and is silicon verified using the 0.18µm CMOS technology. Since the multimodulus 32/33/47/48 prescaler has maximum operating frequency of 6.2 GHz, the values of P- and S-counters can actually be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing.. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S-counter and consumes a power of 0.96 and 2.2 mW in 2.4 and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.
REFERENCES


